IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Robert B. Ogle, Jr. et al.**	Art Unit: 2893
Serial No.: 09/591,266	Examiner: Chen, Jack S. J.
Filed: June 9, 2000	
For: **Anti-Reflective Interpoly Dielectric**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1-7. The Final Rejection issued on August 3, 2009. A notice of appeal and petition to revive the present application was filed in the present application on March 18, 2010. The petition to revive was granted on June 9, 2010, resulting in a two-month period of time to file the present Appeal Brief, which is extendible for an additional five months; thus, the last date to file an Appeal Brief expires on January 9, 2011. This Appeal Brief is being timely filed on November 3, 2010.

REAL PARTY IN INTEREST

The real party in interest is Spansion LLC.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1-15 were originally filed in the present application.

Claims 8-15 were canceled by previous amendment.

Claims 1-7 are pending in the present application.

Claims 1-7 have been finally rejected in a Final Rejection dated August 3, 2009. This Appeal is directed to the rejection of claims 1-7 which appear in the attached "Appendix of Claims on Appeal."

STATUS OF AMENDMENTS

No claim amendments have been entered after issuance of the Final Rejection of August 3, 2009.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1

Independent claim 1 describes a flash memory device. *See*, e.g., page 3, lines 3-11 of the present application. The flash memory device (e.g., the flash memory device shown in Figure 2) includes a substrate (e.g., substrate 42, in Figure 2; *and see id.*, e.g., at page 3, lines 3-11), at least one core stack (e.g., core stack 40, in Figure 2; *and see id.*, e.g., at page 3, lines 3-11), at least one source region adjacent to the at least one core stack (e.g., source region 54 adjacent to core stack 40, in Figure 2; *and see id.*, e.g., at page 4, lines 7-11), and at least one drain region adjacent to the at least one core stack (e.g., drain region 56 adjacent to core stack 40, in Figure 2; *and see id.*, e.g., at page 4, lines 7-11). *See id.*, e.g., at page 3, lines 3-11 and page 4, lines 1-11 with Figure 2. The at least one core stack includes a tunnel oxide layer on the substrate (e.g., tunnel oxide layer 44 on substrate 42, in Figure 2; *and see id.*, e.g., at page 3, lines 3-17), a first polysilicon layer on the tunnel oxide layer (e.g., first polysilicon layer 46 on tunnel oxide layer 44, in Figure 2; *and see id.*, e.g., at page 3, lines 3-17), an anti-reflective interpoly layer atop and in contact with the first polysilicon layer (anti-reflective interpoly layer 48 atop and in contact with first polysilicon layer 46, in Figure 2; *and see id.*, e.g., at page 3, lines 3-17), and a transmissive second polysilicon layer on the anti-reflective interpoly layer (e.g., transmissive second polysilicon layer 50 on anti-reflective interpoly layer 48, in Figure 2; *and see id.*, e.g., at page 3, lines 3-17). *See id.*, e.g., at page 3, lines 3-17 with

Figure2. The anti-reflective interpoly layer (e.g., anti-reflective interpoly layer 48, in Figure 2; *and see id.*, e.g., at page 3, lines 12 through page 4, line 6) has an index of refraction *n* and a thickness *d* and is configured for use with light of wavelength λ_1, such that *d* is an odd numbered multiple of approximately $\lambda_1/4n$. *See id.*, e.g., at page 3, line 12 through page 4, line 6, with Figure2.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-7 under 35 U.S.C. § 102(b) as being unpatentable for anticipation over U.S. Patent Number 5,780,891 to Kauffman et al. (hereinafter "Kauffman").

B. Claims 1-5 and 7 under 35 U.S.C. § 102(b) as being unpatentable for anticipation over U.S. Patent Number 5,888,870 to Gardner et al. (hereinafter "Gardner").

C. Claim 6 under 35 U.S.C. § 103(a) as being unpatentable for obviousness over Gardner.

ARGUMENT

A. Rejection of Claims 1-7 Under 35 U.S.C. § 102(b) as Being Unpatentable Over Kauffman

The Examiner has rejected claims 1-7 under 35 U.S.C. §102(b) as being unpatentable for purported anticipation over Kauffman. *See* item 2 of the Final Office Action dated March 19, 2009 (hereinafter "Final Rejection"). For the reasons discussed below, Appellants respectfully submit that the present invention, as defined by independent claim 1, is patentably novel and inventive over Kauffman.

As Appellants have explained before in detail, the present invention is directed to a core stack for a flash memory device that includes an interpoly layer for use in a lithographic patterning process that is purposefully configured to have advantageous anti-reflective properties. *See*, e.g., page 2 lines 16-19 and page 3 lines 3-11 with Figure 2 of the present application. Additionally, in order for the anti-reflective properties of the interpoly layer to be put to advantageous use, the present invention, as defined by independent claim 1, includes a transmissive second polysilicon layer on the interpoly layer that can be configured to be optically transparent to incident lithographic radiation by, for example, varying the chemistry or concentration of dopants, or by using differing formation techniques, as is known in the art. *See id.*, e.g., at page 3 lines 3-11 and page 4 lines 1-11 with independent claim 1, above.

Appellants respectfully submit, as they have done in previous correspondence, that a patentably distinctive difference between the present invention, as defined by

independent claim 1, and the disclosure provided by Kauffman, is the disposition of the anti-reflective interpoly layer relative to a first polysilicon layer of the core stack comprised by the present invention's flash memory device. Moreover, as Appellants have previously noted, independent claim 1 specifically requires that patentably distinguishable structural difference, unambiguously reciting "an anti-reflective interpoly layer atop and in contact with the first polysilicon layer." *See* independent claim 1, above.

In contrast to the structure described and specifically claimed in the present application, the disclosure of Kauffman expressly teaches formation of an intervening silicon dioxide layer between the first polysilicon layer and the anti-reflective interpoly layer. Specifically, Kauffman teaches that first silicon dioxide layer 20 (rather than an anti-reflective interpoly layer) is formed on first polysilicon layer 18. *See* column 3 lines 60-64 with Figure 3 of Kauffman. Subsequently, "oxynitride layer 22 is deposited over first silicon dioxide layer 20," (not first polysilicon layer 18). *Id.* at column 4 lines 1-3. Furthermore, Kauffman is unequivocal in stating that its oxynitride layer 22 is not to be conflated or confused with other interpoly materials. For example, according to Kauffman: "In the present invention . . . the oxynitride film is a separate and distinct compound deposited over the underlying layer of silicon dioxide." *Id.* at column 2 lines 47-50.

Nevertheless, the Examiner has inscrutably adopted an interpretation of the disclosure of Kauffman which is plainly contrary to the aforementioned express teaching. That is to say, despite Kauffman's admonition that oxynitride layer 22 not be conflated

with other interpoly materials, the Examiner has asserted that Kauffman discloses "an anti-reflective interpoly layer 20/22," insisting against the teaching of Kauffman that "the dielectric 22 taken with 20 is considered as the anti-reflective interpoly layer, i.e., the anti-reflective interpoly dielectric is consisting of layers 22 and 20 . . ." *See* item 2 of the Final Rejection.

However, the portions of Kauffman cited by the Examiner in the Final Rejection as support for its own interpretation of Figure 3 not only fail to provide that support, but discredit the interpretation adopted by the Examiner. For example, according to every embodiment disclosed in Kauffman, first oxide layer 20 is formed on polysilicon layer 18, and oxynitride layer 22 is formed on first oxide layer 20. *See* column 3 line 59 through column 4 line 3 with Figures 3 and 4 of Kauffman. In addition, in a preferred embodiment, second oxide layer 24 is formed on oxynitride layer 22. *Id.* at column 4 lines 23-32. Under no circumstances, however, does Kauffman teach or suggest that its oxynitride layer 22 be formed directly on polysilicon layer 18. Consequently, and contrary to the interpretation advanced by the Examiner in the Final Rejection, Kauffman fails to teach or suggest an anti-reflective interpoly layer atop and in contact with a first polysilicon layer, as described by Appellants and specifically required by independent claim 1. Furthermore, by requiring at least one additional intervening layer as compared to the present inventive concepts, Kauffman's structure incorporates additional undesirable costs associated with additional time and complexity of fabrication, which

further places it apart from the inventive concepts conveyed by Appellants' disclosure. *See*, e.g., page 2 lines 12-13 of the present application.

A separate patentably distinctive difference between the present invention and Kauffman is that, as pointed out above, the present invention's second polysilicon layer is explicitly configured to be transmissive to incident lithographic radiation. *See*, e.g., page 3 lines 4-8 of the present application with independent claim 1, above. By contrast, nowhere does Kauffman disclose or suggest a second polysilicon layer configured to be transmissive to incident lithographic radiation, which is consistent with Kauffman's teaching since Kauffman is solely concerned with the dielectric and resistive properties of its structure, not its optical properties. *See*, e.g., column 1 lines 48-57 and column 4 lines 15-20 of Kauffman. Appellants note that while Kauffman specifies a refractory index for portions of its interpoly layer, this reference is simply used as a method to compare dielectric and resistive properties of its interpoly layer structure against that of conventional interpoly layer structures, as known in the art. *See id.*, e.g., at column 4 lines 15-20. Consequently, Appellants respectfully submit that Kauffman fails to disclose or suggest a transmissive second polysilicon layer as specifically required by independent claim 1 of the present application.

Thus, for all of the foregoing reasons, Appellants respectfully submit that at the time the invention defined by independent claim 1 was made, the invention was not anticipated by, nor would have been obvious in light of the disclosure provided by Kauffman. Thus, Appellants respectfully assert that the invention described by

independent claim 1 is patentably novel and inventive over Kauffman and, as such, claims 2-7 depending from independent claim 1 are also patentably novel and inventive over Kauffman for at least the reasons presented above and also for the additional limitations contained in each dependent claim.

B. Rejection of Claims 1-5 and 7 Under 35 U.S.C. § 102(b) as Being Unpatentable Over Gardner

The Examiner has rejected claims 1-5 and 7 under 35 U.S.C. §102(b) as being unpatentable for purported anticipation over Gardner. *See* item 3 of the Final Rejection. For the reasons discussed below, Appellants respectfully submit that the present invention, as defined by independent claim 1, is patentably novel and inventive over Gardner.

As Appellants have explained above, the present invention is directed to a core stack for a flash memory device that includes an interpoly layer for use in a lithographic patterning process that is purposefully configured to have advantageous anti-reflective properties. *See*, e.g., page 2 lines 16-19 and page 3 lines 3-11 with Figure 2 of the present application. Additionally, as explained above, in order for the anti-reflective properties of the interpoly layer to be put to advantageous use, the present invention, as defined by independent claim 1, includes a transmissive second polysilicon layer on the interpoly layer. *See id.*, e.g., at page 3 lines 3-11 and page 4 lines 1-11 with independent claim 1, above.

According to the embodiment of the present invention specifically recited by independent claim 1, such a configuration includes a relationship between the index of refraction "*n*" of the material comprising the anti-reflective interpoly layer and the thickness "*d*" of that layer, such that *d* is an odd numbered multiple of approximately $\lambda_1/4n$, where λ_1 is the wavelength of incident lithographic radiation. *See id.*, e.g., at page 3 line 12 through page 4 line 11.

By contrast to the principles of the present invention, as defined by independent claim 1, the teaching provided by Gardner is silent with respect to any relationship between the dimensions of the material layers utilized in its disclosed memory cell stack and the wavelength of light used for lithographic patterning in its fabrication process. This is unsurprising, however, in so far as the focus, in Gardner, is purely on the electrical properties of the disclosed interpoly materials, to the exclusion of any optical properties possessed by those materials. *See*, e.g., column 2 line 11 through column 3 line 40 of Gardner.

According to Gardner, the invention disclosed by that reference achieves its success by polishing the upper surface of a floating gate polysilicon layer and depositing an interpoly dielectric comprising oxynitride or a relatively high-K ceramic on the polished surface. *Id.* at column 6 lines 46-65. Moreover, the interpoly oxynitride disclosed in Gardner has its thickness optimized so as to resist breakdown while also being sufficiently thin to reduce capacitive coupling of the floating gate to a control gate. *Id.* at column 7 lines 2-10. Thus, Gardner is entirely indifferent to the optical properties

of oxynitride layer, and consequently fails to disclose or suggest an "anti-reflective interpoly layer having an index of refraction *n* and a thickness *d* and being configured for use with a light having a wavelength λ_1, such that *d* is an odd numbered multiple of approximately $\lambda_1/4n$," as described by Appellants and expressly required by independent claim 1.

In addition, as with Kauffman, Gardner also fails to disclose or suggest a second polysilicon layer configured to be transmissive to incident lithographic radiation, which, as explained above, is unsurprising since Gardner is focused only on the electrical properties of its disclosed interpoly materials. *See id.*, e.g., at column 2 line 11 through column 3 line 40. Consequently, Appellants respectfully submit that Gardner, like Kauffman, fails to disclose or suggest a transmissive second polysilicon layer as specifically required by independent claim 1 of the present application.

For the foregoing reasons, Appellants respectfully submit that at the time the invention defined by independent claim 1 was made, the invention was not anticipated by, nor would have been obvious in light of the disclosure provided by Gardner. Thus, Appellants respectfully assert that the invention described by independent claim 1 is patentably novel and inventive over Gardner and, as a result, claims 2-5 and 7 depending from independent claim 1 are also patentably novel and inventive over Gardner for at least the reasons presented above and also for the additional limitations contained in each dependent claim.

C. Rejection of Claim 6 Under 35 U.S.C. § 103(a) as Being Unpatentable Over Gardner

The Examiner has rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable for purported obviousness over Gardner. *See* item 6 of the Final Rejection. However, as discussed above, Appellants respectfully assert that independent claim 1 is patentably distinguishable over Gardner. Thus claim 6 depending from independent claim 1 is also patentably distinguishable over Gardner for at least the reasons presented above and also for the additional limitations contained in the dependent claim.

CONCLUSION

Based on the foregoing reasons, the present invention, as defined by independent claim 1 and claims depending therefrom, is patentably novel and inventive. Thus, for all of the reasons presented above, early allowance of claims 1-7 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
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Date: 11/3/10

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APPENDIX OF CLAIMS ON APPEAL

Claim 1: A flash memory device, comprising:

a. a substrate;

b. at least one core stack, wherein the at least one core stack comprises:

(1) a tunnel oxide layer on the substrate;

(2) a first polysilicon layer on the tunnel oxide layer;

(3) an anti-reflective interpoly layer atop and in contact with the first polysilicon layer, said anti-reflective interpoly layer having an index of refraction *n* and a thickness *d* and being configured for use with a light having a wavelength λ_1, such that *d* is an odd numbered multiple of approximately $\lambda_1/4n$; and

(4) a transmissive second polysilicon layer on the anti-reflective interpoly layer;

c. at least one source region adjacent to the at least one core stack; and

d. at least one drain region adjacent to the at least one core stack.

Claim 2: The flash memory device, as recited in Claim 1, wherein the at least one source region and the at least one drain region are formed by the method comprising the steps of:

a. depositing a layer of photoresist over the substrate and the at least one core stack;

b. illuminating the layer of photoresist with said light;

c. transmitting some of the light through the transmissive second polysilicon layer;

d. preventing the reflection of the light at the anti-reflective interpoly layer;

e. removing part of the photoresist layer; and

f. implanting a dopant into the substrate.

Claim 3: The flash memory device, as recited in Claim 2, wherein the light has an integer number *m* wavelengths incident upon the anti-reflective interpoly layer, and wherein

$$d \cong \frac{(m+\frac{1}{2})\lambda_1}{2n}, \ where \ \ m = 0,1,2...$$

Claim 4: The flash memory device, as recited in Claim 1, wherein $d \cong \frac{\lambda 1}{4n}$.

Claim 5: The flash memory device, as recited in Claim 1, wherein the anti-reflective interpoly layer is made of silicon oxynitride (SiON).

Claim 6: The flash memory device, as recited in Claim 5, wherein the thickness of the anti-reflective interpoly layer is between about 300 to 400 Å thick.

Claim 7: The flash memory device, as recited in Claim 2, wherein the step of depositing the layer of photoresist, deposits the photoresist onto a surface of the transmissive second polysilicon layer.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)